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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: : Docket: YOR919990336US2

Chao-kun Hu et al. : Prior Group Art Unit: 2815

Serial No.: To be Assigned : Prior Examiner: A. Wilson

Filed: Herewith : Date: November 13, 2001

For: REDUCED ELECTROMIGRATION AND STRESSED INDUCED MIGRATION OF Cu WIRES BY SURFACE COATING

# Preliminary Amendment

Commissioner for Patents
Washington, D.C. 20231

Sir:

## In the Specification

Please replace Equation 1 at page 3, line 19, with the following rewritten equation 1:

$$Cu + Pd^{++} \rightarrow Cu^{++} + Pd \qquad (1)$$

Please replace Equation 2 at page 4, line 5, with the following rewritten equation 2:

$$\text{reducing agent} + Me^{n+} + Cu \rightarrow Cu/Me + \text{oxidized form of reducing agent} \qquad (2)$$

Please replace Equation 3 at page 4, line 9, with the following rewritten equation 3:

$$2\,H_2PO_2^- + Co^{2+} + H_20\ldots((..Cu..)) \rightarrow Co + 2HP0_3^{2-} + H_2 + 4\,H^+ \qquad (3)$$

Please replace the paragraph beginning at Page 7, line 7, with the following rewritten paragraph:

--In Fig. 1, integrated circuit chip 10 has a substrate 11 which may be, for example, Si, SiGe, Ge, SOI and GaAs. Substrate 11 may have formed therein , source 16 and drain 17 regions and gate 18 of a typical FET transistor 19. On either side of source 16 and drain 17 regions are recessed oxide regions 21 and 22 on substrate 11. A layer 23 of oxide is formed over oxide regions 21 and 22 and FET transistor 19. A source contact opening is formed layer 23 and filled with metal 25 which is usually tungsten. Layer 23 and metal 25 are planarized by Chemical Mechanical Polishing (CMP). A capping layer 26 of, for example, silicon nitride is formed on the upper surface of layer 23. Layer 27 of dielectric is formed on layer 26 and trenches are formed therein. A liner 28 is formed on the bottom and sidewalls of trenches and then filled with Cu to form lines 29. Layer 27 and lines 29 are planarized by CMP. A capping layer 31 is formed on the upper surface of layer 27 and lines 29. A layer 32 of dielectric is formed on capping layer 31. Via openings are formed in layers 31 and 32 followed by formation of a metal liner 33 and metal such as Cu in the opening to form via 34. Layers 32 and via 34 are planarized by CMP. A capping layer 36 is formed on layers 32 and via 34. A layer 37 of dielectric is formed on capping layer 36. Trenches or openings are formed in layer 37 and capping layer 36. A liner 38 is formed in the trenches in layer 37 and capping layer 36. The trenches are filled with Cu metal to form lines 39. Layer 37 and lines 39 are planarized by CMP. A capping layer 42 is formed on layer 37 and lines 39. Capping layers 26, 31 and 36 are of a different dielectric than the dielectric of layers 23, 27, 32 and 37 which may be silicon oxide, diamond-like-carbon (DLC), fluorinated DLC, poly (arylene ether), SiCOH etc. SiCOH is described in Serial No. 09/107567 filed 6/29/98 now U.S. Patent 6,147,009 which issued Nov. 14, 2000 which is incorporated herein by reference to show one example of a low k (dielectric constant) dielectric. Note that the BEOL is fabricated using a single damascene Cu process, i.e., each Cu layer is individually processed, and the tops of lines 31 amd 39 are interfaced with dielectric 8.--

## R E M A R K S

A arrow has been shown correctly in place of "dashes" and an "a" in Equations 1-3 on pages 3 and 4.

A typographical error has been corrected and the status of a patent application has been updated.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Further favorable action and allowance of the claims is earnestly requested.

Respectfully submitted,
Attorney for the Applicant(s)

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Equation 1 beginning at page 3, line 19, has been amended as follows:

$$Cu + Pd^{++} \text{ [---------à]} \rightleftarrows Cu^{++} + Pd \qquad (1)$$

Equation 2 beginning at page 4, line 5 has been amended as follows:

**reducing agent + $Me^{n+}$ + Cu [-----à] $\rightleftarrows$ Cu/Me + oxidized form of reducing agent**

(2)

Equation 3 beginning at page 4, line 9, has been amended as follows:

$$2\,H_2PO_2^- + Co^{2+} + H_20\ldots((..Cu..)) \text{ [------à]} \rightleftarrows Co + 2HP0_3^{2-} + H_2 + 4\,H^+ \qquad (3)$$

Paragraph beginning at page 7, line 7, has been amended as follows:

In Fig. 1, integrated circuit chip 10 has a substrate 11 which may be, for example, Si, SiGe, Ge, SOI and GaAs. Substrate 11 may have formed therein , source 16 and drain 17 regions and gate 18 of a typical FET transistor 19. On either side of source 16 and drain 17 regions are recessed oxide regions 21 and 22 on substrate 11. A layer 23 of oxide is formed over oxide regions 21 and 22 and FET transistor 19. A source contact opening is formed layer 23 and filled with metal 25 which is usually tungsten. Layer 23 and metal 25 are planarized by Chemical Mechanical Polishing (CMP). A capping layer 26 of, for example, silicon nitride is formed on the upper surface of layer 23. Layer 27 of dielectric is formed on layer 26 and trenches are formed therein. A liner 28 is formed on the bottom and sidewalls of trenches and then filled with Cu to form lines 29. Layer 27 and lines 29 are planarized by CMP. A capping layer 31 is formed on the upper surface of layer 27 and lines 29. A layer 32 of dielectric is formed on capping layer 31. Via openings are formed in layers 31 and 32 followed by formation of a metal liner 33 and metal such as Cu in the opening to form via 34. Layers 32 and via 34 are planarized by CMP. A

capping layer 36 is formed on layers 32 and via 34. A layer 37 of dielectric is formed on capping layer 36. Trenches or openings are formed in layer 37 and capping layer 36. A liner 38 is formed in the trenches in layer 37 and capping layer 36. The trenches are filled with Cu metal to form lines 39. Layer 37 and lines 39 are planarized by CMP. A capping layer 42 is formed on layer 37 and lines 39. Capping layers 26, 31 and 36 are of a different dielectric than the dielectric of layers 23, 27, 32 and 37 [whcih] which may be silicon oxide, diamond-like-carbon (DLC), fluorinated DLC, poly (arylene ether), SiCOH etc. SiCOH is described in Serial No. 09/107567 filed 6/29/98 now U.S. Patent 6,147,009 which issued Nov. 14, 2000 which is incorporated herein by reference to show one example of a low k (dielectric constant) dielectric. Note that the BEOL is fabricated using a single damascene Cu process, i.e., each Cu layer is individually processed, and the tops of lines 31 amd 39 are interfaced with dielectric 8.